**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A multi-bit split-gate (MSG) flash cell comprising:

a semiconductor substrate having a surface region;

a first drain region and a second drain region formed in said surface region;

a plurality of (N+1) stacked gates separated by N select gates (SGs) between said first region and said second drain region, wherein N is any integer more than one;

a first bit line contacting said first drain region;

a second bit line contacting said second drain region; and

a word line contacting said select gate.

2. (Original) The MSG flash cell according to claim 1, wherein said surface region is of first conductivity type.

3. (Original) The MSG flash cell according to claim 1, wherein said first drain region and second drain region are of second conductivity type opposite from said first conductivity type.

4. (Original) The MSG flash cell according to claim 1, wherein said stacked gates comprises a floating gate and a control gate.

5. (Original) The MSG flash cell according to claim 4, wherein said control gate (CG) can be addressed with a different address as a transfer gate (TG).

6. (Original) The MSG flash cell according to claim 3, wherein said floating gate comprises a first polysilicon layer separated from said surface region by a first dielectric layer.

7. (Currently Amended) The MSG flash cell according to claim [[3 or]] 4 or 5, wherein said CG and TG comprise a second polysilicon layer separated from said first polysilicon layer by a second dielectric layer.

8. (Original) The MSG flash cell according to claim 1, wherein said first bit line and second bit line comprise a third polysilicon layer separated from said first polysilicon layer and second polysilicon layer by a third and a fourth dielectric layer.

9. (Original) The MSG flash cell according to claim 1, wherein said word line comprises a fourth polysilicon layer separated from said first polysilicon layer and from second polysilicon layer by said third and said fourth dielectric layers, and from said first and second bit lines by a fifth dielectric layer.

10. (Original) The MSG flash cell according to claim 1, wherein said word line comprises a fourth polysilicon layer separated from said third polysilicon layer by a fourth dielectric layer.

11. (Original) The MSG flash cell according to claim 1, wherein said select gate is shared by adjacent said stacked gates.

12. (Currently Amended) The MSG flash cell according to claim 1, wherein the access of ~~said~~ a ~~first~~ floating gate ~~transistor~~ of one of said stacked gates is through the turn-on of next adjacent said select gate and a floating gate of next adjacent said ~~floating~~ stacked gate.

13. (Original) The MSG flash cell according to claim 1, wherein said word line is oriented generally normal to said first bit line and said second bit line.

14-31. (Cancelled).

32. (New) The MSG flash cell according to claim 1, further comprising a plurality of diffusion regions formed in said surface region, respectively contacting said select gates.

33. (New) The MSG flash cell according to claim 32, wherein said diffusion regions comprise an impurity dosage higher than that of the semiconductor substrate.

34. (New) The MSG flash cell according to claim 33, wherein said diffusion regions and the semiconductor substrate comprise the same conductivity type impurity ions.